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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,373	07/31/2003	Keith Son	5693P290X 5120	
	7590 04/27/2007 PPLIANCE/BLAKELY	•	EXAMINER	
12400 WILSHI			VIDWAN, JASJIT S	
SEVENTH FLOOR LOS ANGELES, CA 90025-1030			ART UNIT	PAPER NUMBER
	,		2182	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		04/27/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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	Application	No.	Applicant(s)			
	10/633,373		SON, KEITH			
Office Action Summary	Examiner		Art Unit			
	Jasjit S. Vidw		2182			
The MAILING DATE of this communication app Period for Reply	pears on the co	over sheet with the co	orrespondence address			
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DOWN THE MAILING DOWN THE MAILING DOWN THE MAILING DOWN THE STATE OF THE MAILING DOWN THE STATE OF THE MAILING DOWN THE MAILING THE M	ATE OF THIS 36(a). In no event, will apply and will ex e, cause the applicat	COMMUNICATION however, may a reply be time copies SIX (6) MONTHS from the become ABANDONED	l. ely filed he mailing date of this communication. D (35 U.S.C. § 133).			
Status		• .				
1) Responsive to communication(s) filed on 01 Fe	<u>ebruary 2007</u> .					
2a)⊠ This action is FINAL . 2b)□ This	This action is FINAL . 2b) This action is non-final.					
	· 					
closed in accordance with the practice under E	Ex parte Quay	<i>le</i> , 1935 C.D. 11, 45	3 O.G. 213.			
Disposition of Claims						
4) ☐ Claim(s) <u>1,3-5,7-18,20-22 and 24-37</u> is/are per 4a) Of the above claim(s) is/are withdraw 5) ☐ Claim(s) is/are allowed. 6) ☐ Claim(s) <u>1,3-5,7-18,20-22 and 24-37</u> is/are rejuted to is/are objected to is/are subject to restriction and/o	wn from consi	deration.				
Application Papers			•			
9)☑ The specification is objected to by the Examine 10)☑ The drawing(s) filed on <u>01 November 2004</u> is/a Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11)☐ The oath or declaration is objected to by the Ex	are: a)⊠ acce drawing(s) be l tion is required	held in abeyance. See if the drawing(s) is obj	e 37 CFR 1.85(a). ected to. See 37 CFR 1.121(d).			
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 						
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	5) Interview Summary Paper No(s)/Mail Da) Notice of Informal P) Other:	ate			

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DETAILED ACTION

Specification

1. The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code. Page 16 of Applicant's submitted specification includes a hyperlink to SFF-8045 documentation. Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. Claims 1, 4, 5, 8, 9,11, 12, 13, 14, 15, 17,18, 20, 21, 22, 25, 26, 28, 29, 30, 31 and 36, are rejected under 35 U.S.C. 103(a) as being unpatentable over Barth et al, U.S. Pub No: 2003/0191872 [herein after Barth] and further in view of Schimke et al, U.S. Pub No: 2002/0174197 [herein after Schimke]
- 3. **As per Claim 1, 5, 18 and 22**, Barth teaches an apparatus including:
 - (a) Disk drive housing [see Fig. 2, elements 200, 210 and 220 Though the figure is labeled as "prior art", Barth's improvement is solely focused on the Adaptor [Fig. 2, element 200] and not the whole system Examiner construes Barth's teaching as follow: Since Barth teaches having a ATA hard disks as its devices (200, 225), it is inherent that the above elements will be stored within some housing] defining a volume large enough to include an ATA disk drive therein [see Barth, Paragraph 0004 Barth teaches having ATA hard disks as its attached devise "Large enough to

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include an ATA disk drive" i.e. Barth's computer system including the above elements]

- (b) Adaptor in said housing [see Abstract, "ATA (Advanced Technology Attachment) controller"], said adaptor including an ATA disk drive coupling element [see Fig. 3, elements 130, 210 and 215, "Parallel Port" & "Serial Port"] and at least two backplane coupling elements [see Fig. 3, elements 305, 210, "Target Interface" & "Source Interface"]
- (c) Programmable switch [see Fig. 3, element 335] coupled to said backplane coupling elements to control selection of one of at least two paths by which the ATA disk drive can be coupled to the backplane [see Paragraph 0026, "...there may be provided a port assignment unit which may be used for switching between the parallel and serial ports"]
- (d) Serial-to-Parallel converter [see Page 4, Claim 14, "...converting serial data to parallel data to enable data to and/or from SATA compliant storage devices"], said serial-to-parallel converter being within said disk drive housing and coupled to said ATA disk drive coupling element [Fig. 3, elements 335, 210 As can be seen, Port Assignment Unit is coupled to serial port], wherein said serial-to-parallel convert is capable of receiving a set of serial ATA disk drive signals from a serial ATA disk operatively coupled to said ATA disk drive and emitting a set of parallel ATA disk drive signals [see above cited Page 4, Claim 14]
- (e) Parallel-to-serial converter in a second one of the at least two paths [see Page 2, Paragraph 0026, "Another function performed by the port assignment unit is that of the parallel/serial converter i.e., it performs conversion of parallel to serial data signals and vice versa"], said parallel-to-serial converter being within said disk drive housing and coupled to said ATA disk drive coupling element [Fig. 3, elements 335, 130 As can be seen, Port Assignment Unit is coupled to parallel port], wherein the said parallel-to-serial converter is capable of receiving a set of parallel ATA disk drive

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signals from a parallel ATA disk operatively coupled to said ATA disk drive and emitting a set of serial ATA disk drive signals [see Page 2, Paragraph 0026]

Barth fails to teach an apparatus wherein the two coupling elements are Fiber Channel coupling elements wherein the Fiber channel backplane is coupled to first and second housing. Schimke teaches the above limitations of having Fiber Channel interfaces coupled to FC backplane [see Schimke, Page 2, Paragraph 0020, "Devices 120-130 are typically peripheral devices such as storage devices with FC interfaces and are coupled to the FC-AL on a backplane provided by hub"].

One of ordinary skill in the art at the time of Applicant's invention would have clearly recognized the advantage of combining teachings of Barth with that of Schimke in order to achieve higher reliability during fail over through the employing Fiber Channel Arbitration Loop interconnection system [Page 2, Paragraph 0020]. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the two teachings in order to achieve higher reliability during fail over through the employing Fiber Channel Arbitration Loop interconnection system [Page 2, Paragraph 0020].

- 4. **As per Claim 9 and 26**, Barth teaches an apparatus including:
 - (a) Disk drive housing [see Fig. 2, elements 200, 210 and 220 Though the figure is labeled as "prior art", Barth's improvement is solely focused on the Adaptor [Fig. 2, element 200] and not the whole system Examiner construes Barth's teaching as follow: Since Barth teaches having a ATA hard disks as its devices (200, 225), it is inherent that the above elements will be stored within some housing] defining a volume large enough to include an ATA disk drive therein [see Barth, Paragraph 0004 Barth teaches having ATA hard disks as its attached devise "Large enough to include an ATA disk drive" i.e. Barth's computer system including the above elements]

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- (c) Programmable switch [see Fig. 3, element 335] coupled to said backplane coupling elements to control selection of one of at least two paths by which the ATA disk drive can be coupled to the backplane [see Paragraph 0026, "...there may be provided a port assignment unit which may be used for switching between the parallel and serial ports"]
- (d) Serial-to-Parallel converter [see Page 4, Claim 14, "...converting serial data to parallel data to enable data to and/or from SATA compliant storage devices"], said serial-to-parallel converter being within said disk drive housing and coupled to said ATA disk drive coupling element [Fig. 3, elements 335, 210 As can be seen, Port Assignment Unit is coupled to serial port], wherein said serial-to-parallel convert is capable of receiving a set of serial ATA disk drive signals from a serial ATA disk drive signals [see above cited Page 4, Claim 14]
- (e) Parallel-to-serial converter in a second one of the at least two paths [see Page 2, Paragraph 0026, "Another function performed by the port assignment unit is that of the parallel/serial converter i.e., it performs conversion of parallel to serial data signals and vice versa"], said parallel-to-serial converter being within said disk drive housing and coupled to said ATA disk drive coupling element [Fig. 3, elements 335, 130 As can be seen, Port Assignment Unit is coupled to parallel port], wherein the said parallel-to-serial converter is capable of receiving a set of parallel ATA disk drive signals from a parallel ATA disk operatively coupled to said ATA disk drive and emitting a set of serial ATA disk drive signals [see Page 2, Paragraph 0026]
- (f) Second switch coupled to said first path and said second path, said second switch being capable of selecting a connection to said ATA disk drive using either said first path or second path [see Page 3, Paragraph 0030]

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Barth fails to teach an apparatus wherein the two coupling elements are Fiber Channel coupling elements wherein the Fiber channel backplane is coupled to first and second housing. Schimke teaches the above limitations of having Fiber Channel interfaces coupled to FC backplane [see Schimke, Page 2, Paragraph 0020, "Devices 120-130 are typically peripheral devices such as storage devices with FC

interfaces and are coupled to the FC-AL on a backplane provided by hub"].

One of ordinary skill in the art at the time of Applicant's invention would have clearly recognized the advantage of combining teachings of Barth with that of Schimke in order to achieve higher reliability during fail over through the employing Fiber Channel Arbitration Loop interconnection system [Page 2, Paragraph 0020]. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the two teachings in order to achieve higher reliability during fail over through the employing Fiber Channel Arbitration Loop interconnection system [Page 2, Paragraph 0020].

- 5. As per Claim 14, Barth as modified by Schimke above teaches an apparatus including all the limitations as addressed above in rejection of Claim 1. Barth fails to however, teach a second housing containing all the same limitations as the first housing taught by Barth. Although, Barth does not disclose a plurality of housing elements including the cited references, the courts have upheld that mere duplication of parts has no patentable significance unless a new and unexpected result is produced (see In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to provide plurality of housing in effect in order to access more than total of three ATA disks at the same time [see Barth, Paragraph 0028].
- 6. **As per Claim 31 and 36,** Barth teaches an apparatus comprising:
 - (a) Adaptor [see Abstract, "ATA (Advanced Technology Attachment) controller"] coupled to a disk drive housing to couple an Advanced Technology Attachment (ATA) disk drive within the disk drive housing to one of a plurality of backplanes [see Fig. 3, elements 130, 210 and 215 ports connecting to ATA or SATA storage devices]

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(b) Serial-to-Parallel converter [see Page 4, Claim 14, "...converting serial data to parallel data to enable data to and/or from SATA compliant storage devices"], wherein said serial-to-parallel convert is capable of receiving a set of serial ATA disk drive signals from a serial ATA disk operatively coupled to said ATA disk drive and emitting a set of parallel ATA disk drive signals [see above cited Page 4, Claim 14]

(c) Parallel-to-serial converter in a second one of the at least two paths [see Page 2, Paragraph 0026, "Another function performed by the port assignment unit is that of the parallel/serial converter i.e., it performs conversion of parallel to serial data signals and vice versa"], wherein the said parallel-to-serial converter is capable of receiving a set of parallel ATA disk drive signals from a parallel ATA disk operatively coupled to said ATA disk drive and emitting a set of serial ATA disk drive signals [see Page 2, Paragraph 0026]

- As per Claim 4, 8, 11, 12, 17, 21, 25, 28 and 29, Barth as modified by Schimke above teaches an apparatus wherein said switch includes an input port capable of receiving instructions [see Fig. 3, elements 325, 330, 340], said instructions being interpretable by a computing device to control said switch [see Barth Paragraphs 0026 and 0027].
- 8. As per Claims 13, 15, 20 and 30, Barth as modified by Schimke above teach an Apparatus wherein said second switch is capable of being coupled to a second switching signal [see Barth Page 3, Paragraph 0030]

9. Claims 3, 7, 10, 16, 20, 24, 27, 33, 34, 35, 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barth, Schimke and further in view of Gallagher et al U.S. Patent No: 6,742,068 [herein after Gallagher]

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10. As per Claims 3, 7, 10, 16, 20, 24, 27, 33, 34, 35, 37 Barth and Schimke teaches the limitations of Claims 1, 5, 9, 14, 18, 22 and 26, however fail to teach an Apparatus wherein each of said fiber channel back-plane coupling elements includes an port capable of being coupled to a power source, whereby said ATA disk drive coupling is capable of receiving input power from a selectable source.

Gallagher however teaches the above limitations of Apparatus wherein each of said fiber channel back-plane coupling elements includes an port capable of being coupled to a power source, whereby said ATA disk drive coupling is capable of receiving input power from a selectable source [see Gallagher, Col. 6, Lines 4-21].

It would have been obvious to one skilled in the art at the time of Applicant's invention to have a power port on the Fiber Channel backplane in order to provide power to the system [see Gallagher, Col. 1, Lines 10-25]. It is for this reason that one of ordinary skill in the art at the time of Applicant's invention would have been motivated to combine the teachings in order to provide power to the overall system [see Gallagher, Col. 1, Lines 10-25].

Response to Arguments

11. Applicant's arguments with respect to claim 1, 5, 9, 14, 19, 22, 26, 31, 36 have been considered but are most in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX

MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should

be directed to Jasjit S. Vidwan whose telephone number is (571) 272-7936. The examiner can normally

be reached on 8am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, KIM

HUYNH can be reached on (571) 272-4147. The fax phone number for the organization where this

application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application

Information Retrieval (PAIR) system. Status information for published applications may be obtained from

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1000.

JSV 4/16/07

KIM HUYNH

SUPERVISORY PATENT EXAMINER

4/18/07